Update on Tagger Microscope Prototyping

for the GlueX Collaboration Meeting: January 2010

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Electronics Overview

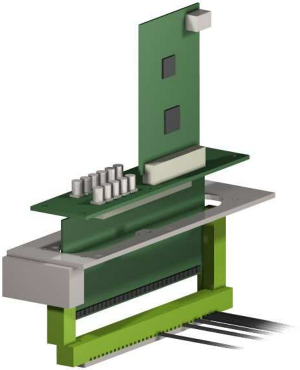
Control board:

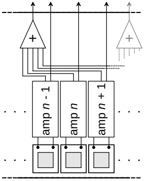
- Firmware loaded on FPGA
- Ethernet communication with PC
- V_{bias} via DAC: 32-chan., $14\,\mathrm{bit}, \lesssim$ 200 V
- on-board health sensors (Temp., ADC) of self and amp. board

Backplane: power; patch through of SiPM signals, bias voltage, monitor line

Amplifier boards contain:

- array of up to 30 SiPMs
- fast, two-stage transimpedance amplifiers
- summing circuitry
- board temperature sensor ($\pm 0.5\,^{\circ}\mathrm{C}$)

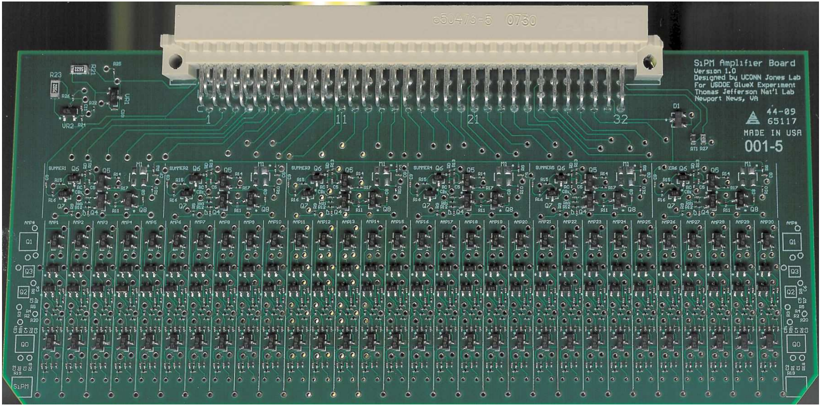




SiPM Amplifier Board

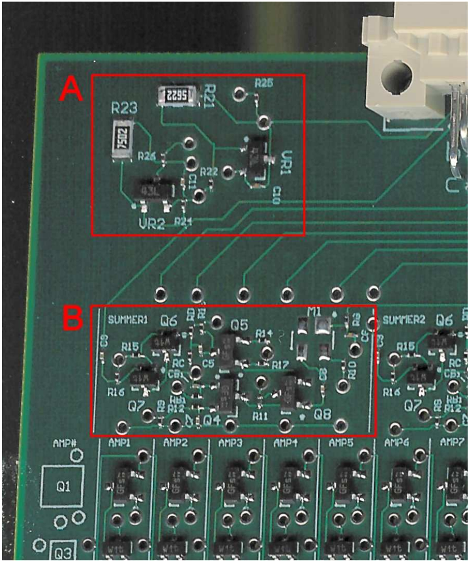
Amplifier Board prototypes have been received!

- awaiting receipt of the mating board (Backplane)



(Mitchell "Woody" Underwood)

Amplifier Board Features

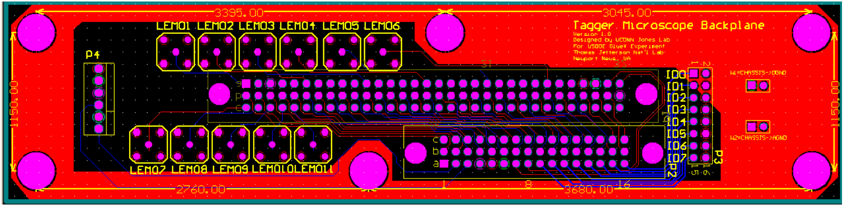


A. Voltage references circuits (with large resistors for easy tweaking)

B. Summing circuit instance, adding signals from the 5 amps below equipped with gain selection

Status of Backplane

The Backplane **board prototype is complete** and will be received soon, pending processing of purchase order (paperwork got stuck somewhere in the university bureaucracy)



Review of board's functions:

- Control/Amp board patch-through with good light-seal
- power distribution
- analog output (LEMO connectors for wiring to fADC)
- 8-bit board address coding via jumpers

Digital Control Board Prototypes

3 assembled Control Boards were received last summer.

- a few cases of layout mistakes have been caught and corrected.
- clock compatibility issue has been solved with a new clock source.
- 2 boards produce overload on low voltage supply lines to DAC (Ball Grid Array!)
  - current hypothesis: improper temperature profile used in reflow process
  - returned to assembly firm for x-ray imaging.
- Firmware debugging is complete:
  - non-DAC-related functionality tested on all boards.
  - **the healthy board is operational and meets all specs!**

Control Software

Control software is in development. *(Michael Fowler)*

Overall software structure:

1. Microscope control boards: FPGA firmware ✓

   $\Updownarrow$ ethernet

2. C++ based packet parser/writer based on `libpcap` - encapsulates the protocol ✓

   $\Updownarrow$ sockets

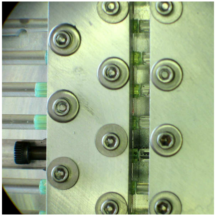
3. Java-based control tools [in progress]
4. GUI [in progress]

Integration into a larger suite of control software will be straightforward.

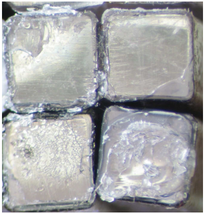
Optical Epoxy Approach

Conveyor belt assembly of fibers well established:

- End-milling streamlines trimming and polishing
- Trapped bubbles in cured epoxy eliminated: quick vacuum treatment before application
- Batch gluing of scintillator to waveguide is now easy; results consistent
- Fiber curl reshaping and packing into bundles, thin isolation coats worked out

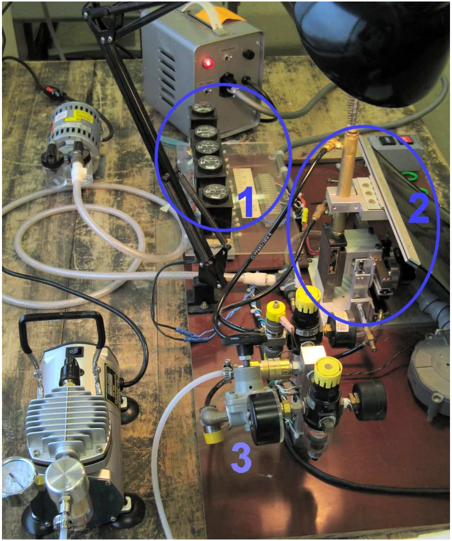


Problem: the optical glue bonds are weak and brittle (broken joint below)
Possible solution: improving bonding to fiber by leaving rougher surface.



(Brendan Pratt, Jim McIntyre)

Fusing Fibers

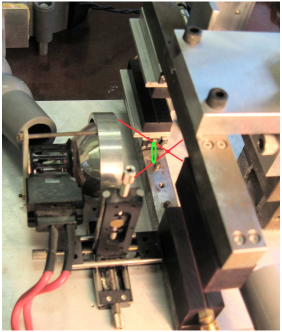


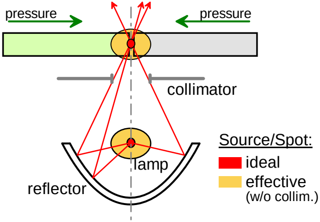
Fiber splicer designed in MSU by Ron Richards (for GEM and DØ)

1. timing relays to automate steps
2. splicer
3. pneumatic control valves, indicators etc.

Our initial concern: the acrylic cladding has a much lower melting point than polystyrene. Would the former mix, melt/burn away?

Splicing Details





Essential features of the splicing jig

- A $250\,\mathrm{W}$ photo lamp heats the joint
- A collimating foil (with aperture indicated in green) produces a roughly focused spot at fiber joint
- Twin clamps with grooves for fibers; the clamp in background applies pressure along fiber axis during welding
- Air-cooled glass ferrules (not shown) mold the melting plastic near junction

Fiber Splicing Tests

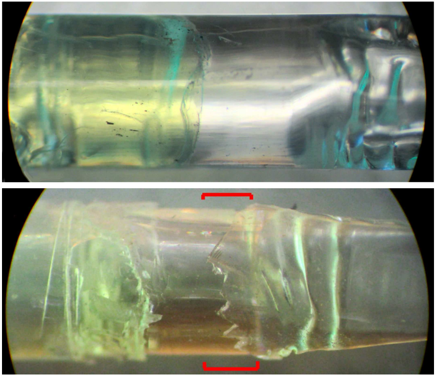


Figure. Square fibers welded in a cylindrical ferule for an initial test.

Bottom photo shows results of efforts to chip off cladding.

(Brendan Pratt)

Very promising early tests of the apparatus: without proper molding ferrules for square fibers or tuned beam time/focus

- Excellent bond and apparent optical clarity
- Distinct cladding layers preserved! (Note remains after flaking off cladding - bracketed in red above)

Goals for Beam Test

Preliminary tests on the bench of all the control and readout functions will be conducted. A pulser can be used for much of the initial testing.

Issues to look into during beam test

- testing amplified SiPM signals with fADC (if available)
- practice online scintillator alignment to electron trajectory
- pulse photo-statistics: satisfying time resolution requirement?
- pulse shape: efficiency lost due to dead time.
- any rate-related issues in SiPMs
  (hopes to push the detector to $5\,\mathrm{MHz}$)
- cross-talk - signal sharing among...
  - adjacent optical channels.
  - adjacent amplifiers

  (Tolerable? Consistent with the Monte Carlo?)

Outlook

Tentative work schedule on the prototype for the next few weeks:

1. testing the full complement of electronics pending receipt of backplane
2. minimal interface software (i.e. w/o GUI, record-keeping etc.): $\sim$ 2 weeks
3. mechanical fabrication/assembly: $\sim$ 3 weeks
4. fiber array fabrication: 1-3 months (depends on success fusing fibers)
5. Expected beam test: Hall B, (parasitically with g9 Frost)
   aim: March 2010 - start of run, possibly later in the spring.