Contents

Chapter 7

Readout Electronics

7.1 Overview

The goal of the GLUEX readout electronics system is to digitize and read out the detector signals for level 1 trigger rates of up to 200 *kHz* without incurring deadtime. A pipelined approach is required. The digitized information will be stored for several *μs* while the level 1 trigger is formed. Multiple events must be buffered within the digitizer modules and read out while the front ends continue to acquire new events.

A summary of the GLUEX detector subsystems from an electronics viewpoint is shown in figure 7.1.

Two basic types of readout electronics will be used in GLUEX, FADCs and TDCs. Detectors which measure energy will be continuously sampled with flash ADCs while detectors which require precise time measurements will use a multi-hit TDC. No currently available commercial solutions exist. These boards will be designed by our collaboration. Prototypes have been constructed, and are being tested.

The number of channels in the GLUEX detector is not large enough to justify the financially risky development of custom integrated circuits. ICs developed for other experiments will be used as well as commercially available chips. Programmable logic devices will be extensively used for data path, memory, and control functions.

Technology is constantly evolving, and the optimum solution for the GLUEX detector depends on when funding becomes available and the construction schedule. Presented here is a preliminary design which could be implemented with currently available components.

Figure 7.1: Detector subsystems

7.2   FADCs for Calorimetry

The calorimeters will be read out with 8-bit, 250 *MHz* FADCs. The 250 *MHz* sampling clock will be derived from the 1499 *MHz* accelerator clock. This sampling rate and bit depth is well matched to the FEU84-3 PMTs used in the Forward Calorimeter, and is adequate for the silicon PMTs used in the Barrel Calorimeter. Additional FADC channels will read out the Photon Tagger, Backwards Veto, Start Counter, Čerenkov Detector, and time-of-flight PMTs.
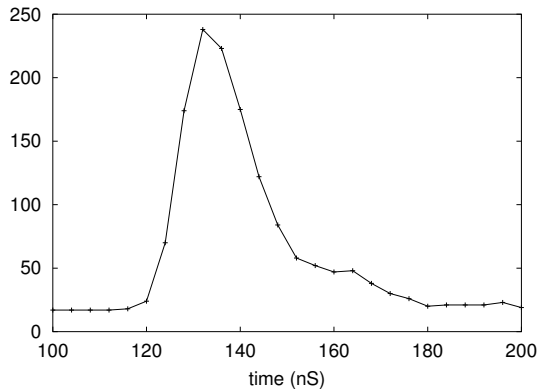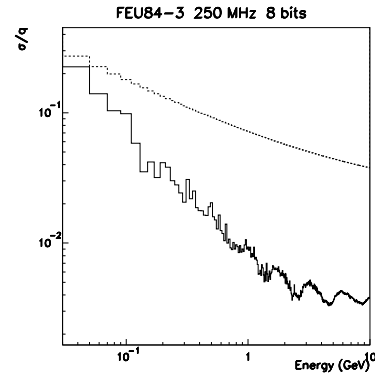

Figure 7.2: Digitized FEU84-3 pulse.

Figure 7.3: Dashed - calorimeter resolution, Solid - FADC resolution.

Figure 7.2 shows an FEU84-3 PMT pulse digitized by the prototype FADC described in section 7.2.1. Note that the sum of the samples from 120 to 180 *ns* is 1429; for this PMT the 8-bit FADC is equivalent to a 10 or 11-bit conventional charge-integrating ADC. To address resolution concerns, simulations were performed to show that the proposed FADC provides an adequate measurement. Pulses measured with a digital ocilloscope were fitted to determine their functional form. The response of the FADC was simulated using this functional form and the time integral of the function was compared to the summed output of the simulated FADC for many pulses. Since the relationship between deposited energy and pulse height in this type of calorimeter is known, direct comparison of the resolution due to the FADC and the resolution of the calorimeter is possible. Figure 7.3 shows the result of this comparison. Clearly, above 0.15 *GeV* the resolution of the FADC is small compared to the intrinsic resolution of the calorimeter.

The FADCs will also give a measurement of the time a photon arrived at the calorimeter. Previous work [1, 2] indicates that a time resolution better than the FADC sampling interval can be achieved by fitting the FADC waveform.

To study how well this time could be determined a "library" of pulses from phototubes of the type to be used was created using a digital ocilloscope with a 2.5 *GHz* sampling frequency. The leading edge of these sampled pulses were fitted to a 9th order polynomial to determine the location of various "features" of the pulses. The features considered were the time the pulse achieved 10, 25, 50, 75, 90 and 100% of its maximum value. These features carry the arrival time information of the pulses and were used as reference times.

To determine how well the FADC could determine the pulse arrival time, the samples from the digital ocilloscope (2.5 *GHz*) were averaged over 10 samples (to 250 *MHz*) and quantized to 8 bits. These transformed samples are what would be expected from the FADC system proposed here. Using only the bin containing the pulse maximum and the two samples preceeding it and a simple algorithm, it was found that the 50% crossing time could be determined with a resolution of 160 *ps* compared to the time determined by the detailed fitting described above. This resolution is sufficent to determine if a pulse is in time with an event (rejecting background) or to determine the time of the event sufficiently well to select the beam "bucket" that initiated the event.

7.2.1 Prototype

A single channel prototype of the calorimeter FADC has been designed and built at Indiana University. A block diagram is shown in Fig. 7.4 and a photo in Fig. 7.5.
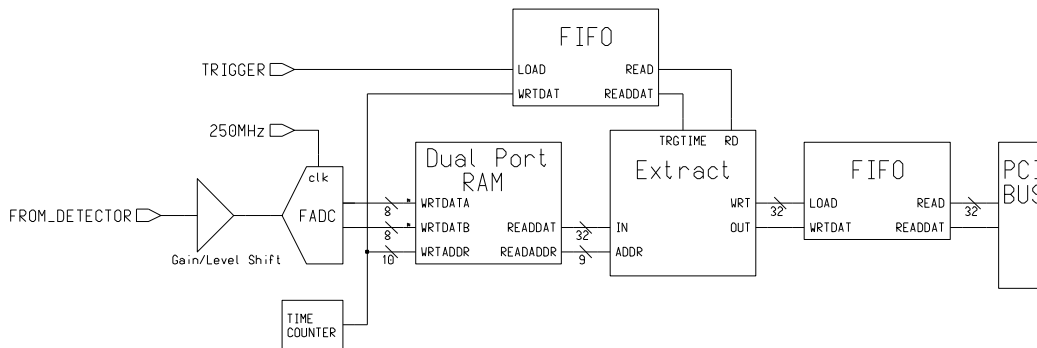

Figure 7.4: Block diagram of prototype FADC board.

A differential amplifier inverts the negative PMT signal and shifts the voltage levels to match the input range of the digitizer integrated circuit. The digitization is performed by an SPT7721 integrated circuit manufactured by
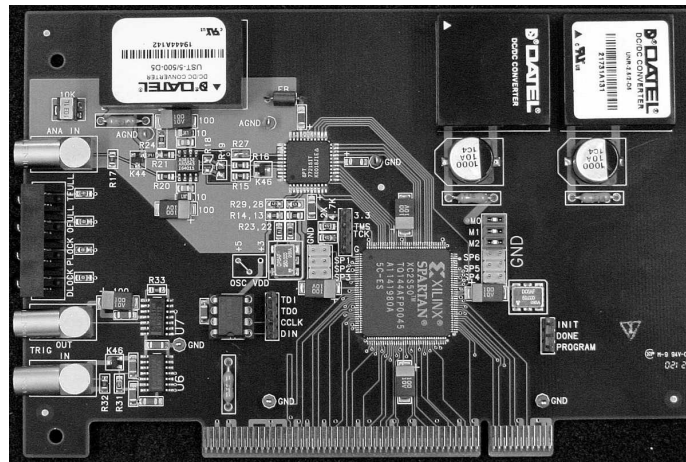
Figure 7.5: Photograph of prototype FADC board.

Fairchild Semiconductor [3]. This IC costs about US$20. An 8-bit value is produced internally every 4 ns; two samples are output every 8 ns (125 MHz).

All digital functions are performed in a Xilinx [4] XC2S50 programmable gate array. This IC costs about US$10. A dual port RAM configured as a circular buffer stores the data for 8 microseconds. Upon receipt of a trigger signal the data from the time window of interest is copied to an output FIFO which can buffer the data from multiple events. This FIFO is interfaced to a 32 bit, 33 MHz PCI bus. More information on this prototype is available [5].

7.2.2   Additional requirements for final version

The final version of the calorimeter FADC board will include pipelined adders operating at the 125 MHz digitizer output clock which continuously sum the digitized information from all channels on a board. Additional pipelined adders will sum the information from all boards in a crate, and then sum the information from all the crates associated with a detector. The sum of all channels will be passed through a shift register giving a time history. Successive samples within a programmable time window will be summed, analgous to the gate in a conventional charge sensitive ADC. Energy sums from the Forward and Barrel Calorimeters will be used in the level 1 trigger. A block diagram is shown in Fig. 7.6.

Assuming a 100 ns time window, each FADC channel will produce 25 bytes of data per level 1 trigger. In the final version of the FADC we will want to suppress the readout of channels with no data. The FADC data will be processed in real time to provide an energy and time measurement. We believe
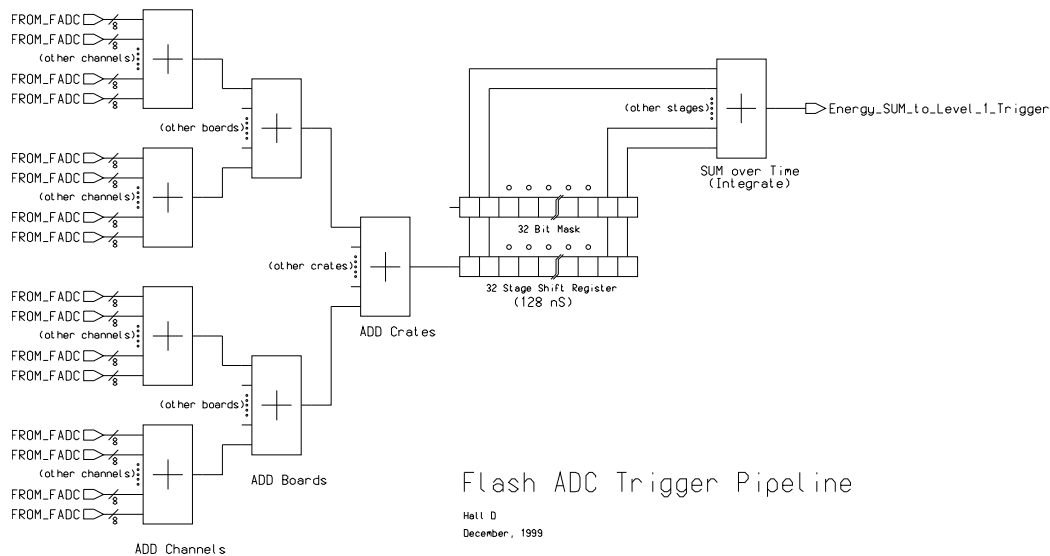
Figure 7.6: Block diagram of energy sum.

that the raw FADC data can be reduced to about 10 bytes per channel. This zero suppression and pulse shape processing may be done at the channel level in the gate array, at the board level, the crate level, the detector system level, or in some combination of these levels.

7.3 FADCs for Tracking

The Central Tracking Drift Chamber anodes will be read out with 10 or 12-bit, 125 *MHz* FADCs. The additional dynamic range is required for the dE/dx measurement. The Forward Tracking Drift Chamber cathodes will be read out with 10 or 12-bit 62.5 *MHz* FADCs. The exact read out electronics requirements for these detectors is the subject of ongoing R&D efforts.

7.4 TDCs

The Photon Tagger, Start Counter, Forward Drift Chamber anodes, Čerenkov Detector, Barrel Calorimeter, and Time of Flight detectors will be read out by multi-hit TDCs.

7.4.1 Jefferson Lab TDC

A high resolution pipeline TDC module has been developed for use at Jefferson Lab. The design is targeted to meet the requirements of current experiments, as well as to serve as a prototype for future experiments at Jefferson Lab, including Hall D. The design is implemented as a VME-64x module. This bus standard was chosen because it is already in use at Jefferson Lab, has good (and evolving) data transfer capabilities, and reasonable channel densities are possible.

The module is built around the TDC-F1 integrated circuit from acam-messelectronic gmbh [6]. The TDC-F1 chip was designed for the COMPASS experiment at CERN [7], and costs about $130 each in small quantities. The chip utilizes purely digital delay techniques to measure time. In normal mode the TDC-F1 chip provides 8 input channels with resolution of 120 ps (LSB). In high resolution mode channels are combined in pairs to yield a resolution of 60 ps for 4 input channels. The dynamic range for measurement is 16 bits. The resolution of the chip is tunable about its nominal value. A PLL circuit adjusts the core voltage of the chip to compensate for temperature and supply voltage variation, assuring stability of the resolution value. On-chip buffering for input channels, triggers, and output data allows for multihit operation with nearly zero deadtime. The chip also has a complex trigger matching unit that can filter out hits unrelated to the input trigger. When enabled, only hits that are within a programmed timing window and latency from the trigger time are kept. The trigger matching feature is used in common start and synchronous measurement modes. In common start mode, an external start signal resets the internal measurement counter and a delayed trigger signal sets the measurement window. In synchronous mode, an external 'sync reset' signal is used to reset the internal measurement counter and clear internal buffers. Internal start signals are then automatically generated at a programmable rate.

Figure 7.7 shows a block diagram of the TDC module. The 8 TDC-F1 chips on the module provide 64 channels in normal mode, or 32 channels in high resolution mode. Front panel input signal levels are differential ECL to be compatible with existing systems a Jefferson Lab. Timing control signals are also available through backplane connections for ease of system integration. A 128K word deep FIFO is attached to each TDC-F1 chip to buffer its output data. In addition, a global 1K word FIFO buffer is implemented within the single FPGA that controls the module. The external RAM shown in the figure is not present on this version. The module can be set up to interrupt the crate controller after a programmable number of triggers have been received.
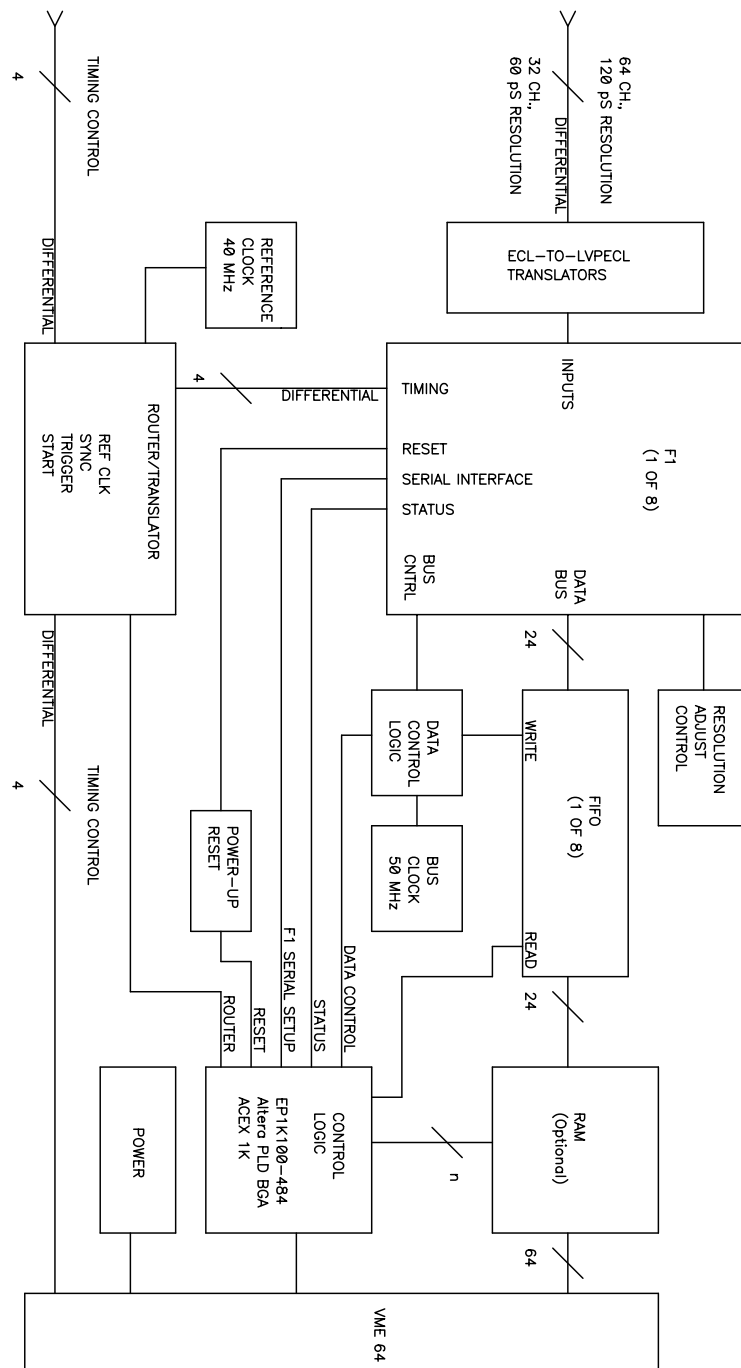
Figure 7.7: Block diagram of TDC board.

During read out the module will provide a block of data associated with a pro-
grammed number of triggers, and then terminate the transaction. To enhance
system performance a set of TDC modules may be read out as a single logical
read using a multiblock read protocol. This involves passing a token between
modules along a private daisy-chain line. In this setup, only the first module
in the chain will generate the interrupt, and only the last module in the chain
will terminate the transaction. Configuration parameters for the 8 TDC-F1
chips are stored in non-volatile memory on the module and may be updated
by the user. The configuration process is automatic at power up.
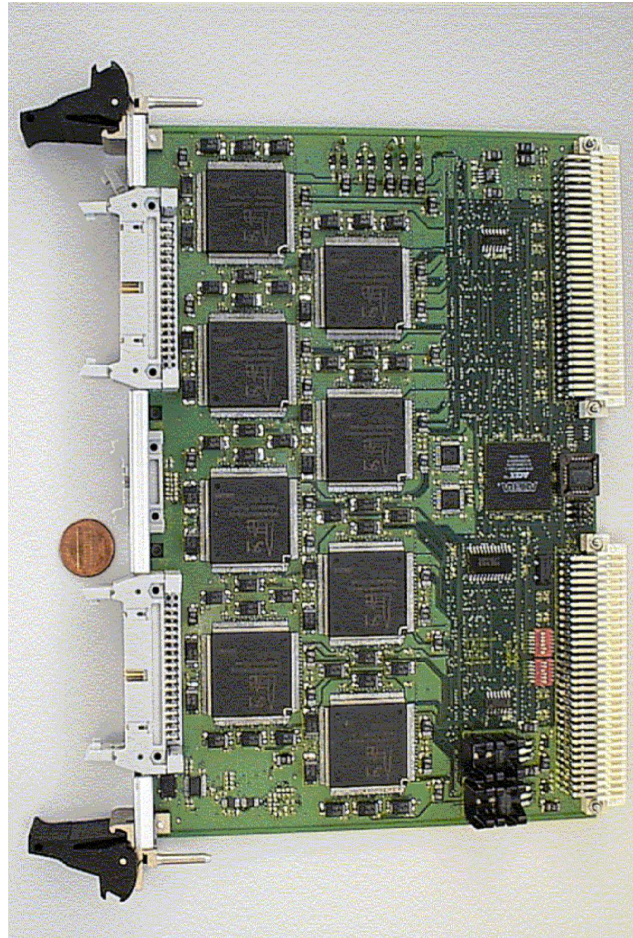

Figure 7.8: Photograph of TDC board.

A photograph of the module is shown in Figure 7.8. Fifty TDC mod-
ules have been produced and are currently being installed into Jefferson Lab
experiments in Halls B and C.
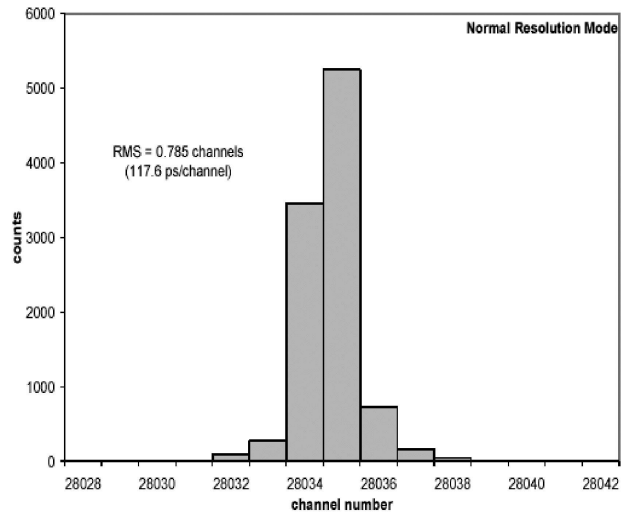
Figure 7.9: TDC performance in low resolution. (resolution=86.2ps)

Figure 7.10: TDC performance in high resolution. (resolution=61.2ps)

7.4.2   TDC Performance

Figure 7.9 shows the timing distribution for an input signal that has a fixed
time relationship to the start signal. The TDC was operated in high resolution
mode. Unfolding the uncertainty of the input signal (33 ps) from the measured
distribution yields a TDC resolution (RMS) of 61.2 ps.   Figure 7.10 shows

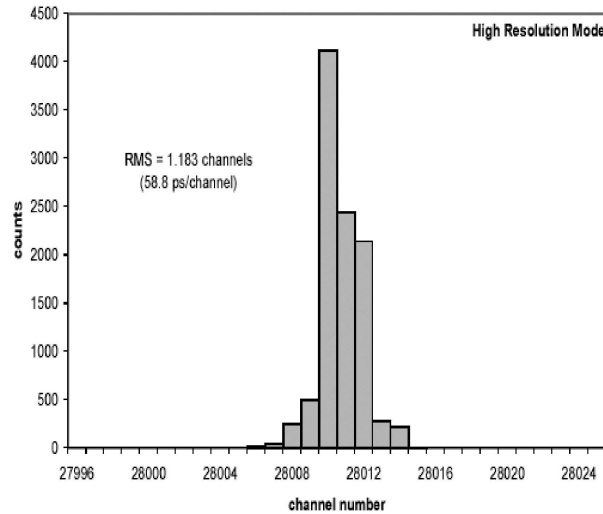the equivalent distribution for a TDC operated in normal resolution mode. The resolution is 86.2 ps. These resolutions were confirmed across the entire dynamic range of the TDC, and for trigger rates up to 200 KHz. Full crate tests have been performed using the multiblock readout protocol. Sustained data transfer rates of 40 Mbytes/s over the VME bus have been achieved.

7.4.3   Additional requirements for final version

A 62.5 *MHz* clock phase-locked to the accelerator will be distributed to all TDC modules so that every channel has the same time calibration. With this clock frequency, LSB resolutions will be 125 *ps* for the standard version and 62.5 *ps* for the high resolution version.

A commercial TDC module, the CAEN[8]v1290, based on the HPTDC chip developed at CERN, is being evaluated by Jefferson Lab. It might be possible to use this type of TDC to provide 31 *ps* LSB resolution for the time-of-flight counters.

7.5   Track Count

The Start Counter, Barrel Calorimeter, and Time of Flight detectors will require pipelined adders to implement a track count for use in the level 1 trigger.

7.6   Clock Distribution and Pipeline Synchronization

A 62.5 *MHz* global front end clock will be phase-locked to the 1499 *MHz* accelerator clock. This global clock will be distributed to all readout electronics crates and used directly by the TDCs and Forward Drift chamber cathode FADCs. The Calorimeter and Central Drift chamber FADCs will phase-lock their higher frequency clocks to the global front end 62.5 *MHz* clock. A global reset will be distributed to synchronize all pipelines. The level 1 trigger as well as calibration and other special triggers will also be distributed globally.

7.7   Discriminators and Amplifiers

Detectors which provide precise timing (Photon Tagger, Start Counter, Barrel Calorimeter, and Time of Flight counters) will require "constant fraction"

discriminators. The Forward Drift Chamber anodes require leading-edge discriminators mounted on the chambers inside the solenoid. The Central Drift Chamber anodes and Forward Drift Chamber cathodes will need an amplifier to drive their FADC inputs. These amplifiers should be located on the chambers. ICs developed for the Atlas [9] detector are being considered for all chamber mounted electronics.

7.8 High Voltage

The Forward Calorimeter PMTs will be powered by Cockcroft-Walton voltage multipliers [10] which will be built at Indiana University. This type of base provides for the very low power consumption necessary for such a tightly packed array and is controlled over a CAN communication link. One hundred prototypes of these bases have been built at Indiana University and are being tested. The other GlueX PMTs will likely use conventional resistive divider bases powered by commercial HV power supplies. The Tracking Chambers will use commercial HV power supplies with sensitive current monitoring.

7.9 Packaging

The calorimeter FADC circuit requires about 50 cm^2 of board space and adjacent channels will need to be about 2 - 3 cm apart. This implies a density of about 8 channels on a 6U board or possibly 16 channels on a 9U board.

The tracking FADCs will be designed at Jefferson Lab. Sixteen channels of 125 MHz FADC for the Central Drift chamber should fit on a 9U board. The exact requirements for the Forward Drift cathode FADCs have not been determined; it should be possible to put 64 channels of 62.5 MHz FADC on a 9U or possibly even a 6U board.

In the low resolution (125 ps) version of the TDC 64 channels fit on a 6U board. This version of the TDC is used for the Forward Drift Chamber anodes.

The Photon Tagger, Start Counter, Barrel Calorimeter, and Time of Flight counters require the high resolution (62.5 ps) version of the TDC; the density is 32 channels per 6U board.

Assuming a maximum of 18 boards in a crate, and 3 9U or 4 6U crates in a 7 foot tall rack, figure 7.11 summarizes the space required for the readout electronics. Estimated counts for high voltage, gas handling, level 1 trigger, and other necessary racks are also included.

The readout electronics will be located as close to the detector as possible to minimize signal cable runs. Note that the Tagger electronics will be be

Figure 7.11: Rack space

located in a separate building 80 *m* upstream of the main detector. The Time of Flight and Forward Calorimeter electronics will be downstream of these detectors. Cabling from detectors inside the solenoid will exit at the upstream and downstream ends of the magnet and connect to nearby electronics. Fiber optic cables will transport the data from the crate readout processors to the level 3 trigger processor farm in the GLUEX counting house.

7.10   Readout Bus

FASTBUS crates are no longer being manufactured, and FASTBUS is not being considered for GLUEX. CAMAC crates are fairly slow and have limited board space and power available. Some legacy devices like discriminators, trigger logic or HV supplies which are not part of the data readout may be packaged in CAMAC, but not the bulk of the readout electronics.

VME is popular at Jefferson Lab and the TDC prototype is constructed on a VME64x card. Compact PCI is used extensively in the telecommunications industry and can be driven directly by typical FPGA ICs without the need for bus interface ICs. Predefined PCI interface "cores" are available, minimizing design time. One disadvantage of cPCI is that bridges are required for a system with more than 8 slots, although commercial bridges which consume no slots are available. VXI and PXI are "instrumentation" extensions to VME and cPCI. Shielding, triggering, clock distribution, and additional power are added to the basic bus standard.

The FADCs require a low skew fanout of the 250 *MHz* clock, a synchronization signal, and the level 1 trigger. The need to form a digital global energy sum for the level 1 trigger will probably drive the choice of packaging for the calorimeter FADCs. Some sort of custom backplane will be required to support the trees of adders which form the energy sum and track counts.

The telecommunications industry is moving towards "Switched Serial Fabrics." This adds a high speed serial connector to the backplane which can support Ethernet and other high speed serial technologies. For VME the applicable standard is VXS (VITA 41) and for cPCI the standard is cPSB (PICMG 2.16). For a 16 channel FADC module producing 25 bytes per channel per level 1 trigger; a level 1 trigger rate of 200 *kHz*; and a 2% occupancy the data readout bandwidth required for a module is 16 Megabits per second, well within the capability of a 100baseT Ethernet connection.

7.11 Construction

Indiana University has experience building large electronic systems for experiments at Fermilab, Brookhaven, and Jefferson Lab. The GLUEX experiment is larger and more complex than past experiments and will require the development of new techniques. High reliability is crucial to the success of the GLUEX experiment. We plan to begin long term tests of GLUEX electronics as soon as they are produced giving early identification of problems and failure modes.

Figure 7.12: Selective assembly robot.

A robotic electronic assembly machine[11] shown in figure 7.12 was purchased and used to construct 100 prototype Forward calorimeter Cockcroft-Walton PMTbases. This device dispenses solder paste, picks and places components, and uses infrared lasers to selectively solder components without disturbing nearby devices. This facilitates building a board in stages and testing partial assemblies, a technique especially useful in producing the Cockcroft-Walton PMT bases. The infrared lasers are particularly useful for removing and replacing defective components.

Producing electronics assemblies in house has several advantages over having a commercial firm doing the assembly. To achieve the lowest cost, a commercial service would assemble a large batch all at once. This risks learning about problems after it's too late to change anything. Assembling smaller batches in house allows immediate feedback to the assembly process.

The lifetime of the GLUEX experiment will be long enough that we must plan for maintenance and repair of the custom electronics. Sufficient spare parts must be purchased at construction time to avoid the risk of a component manufacturer discontinuing some crucial part. Spreading the purchase of components over too long a time also risks some components becoming unavailable.

Jefferson Lab used a commercial board assembly contractor to build the 50 TDC boards used in Hall C. No major problems were associated with this contract assembly, although it was necessary to quickly test the first few units before committing to assembling the remainder.

7.12 Review

The GLUEX electronics were reviewed by one internal and two outside reviewers in July of 2003. The report of this review is attached as an appendix. The review was scheduled at an early stage in the development of GLUEXso that their recommendations could be incorporated into final designs. The guidance of the committee has been extremely useful in the continued prototyping and design of the system.

The present design for the GLUEX electronics differs in a few ways from the reviewers recommendations:

> At the time of the review it was believed that a single FADC module could be used for all detectors. The detector characteristics have been further defined since the review and it seems unlikely that one type of FADC is optimal for all detectors. The channel count for the Forward drift cathodes has grown substantially; the overall system cost will likely be lowered by designing a module specifically for this detector. The different types of FADC will be as similar as possible; it may be possible to use a common printed circuit board stuffed with different components.

> The reviewers recommended locating the readout electronics in a radiation free area. The collaboration believes the advantages of shorter signal cables outweigh the access considerations and is planning to locate the electronics in crates adjacent to the detector. Access to the above ground GLUEX detector should be easier than access to the existing underground experiments at Jefferson lab.

List of Figures

List of Tables

Bibliography

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