Appendix C

Report of the Hall D Electronics Review Committee

Review Committee:

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We have organized the report as a response to the questions posed in the charge to the committee.

Is the GlueX electronic design sound?

Although the GlueX electronics design has many features that differ from present JLab experiments, the design is fairly conventional relative to many other recent nuclear and high energy physics experiments. The GlueX electronics design is characterized by:

- Detector-mounted analog front-end electronics
- Pipelined data acquisition
- Crate-based TDC and Flash ADC modules
- Two stage trigger, with a hardware-based first level followed by software-based second level
- Parallel event building

All of these characteristics are sound and appropriate choices for GlueX (where "appropriate" assumes adequate human and fiscal resources). Although the GlueX electronics design parameters (e.g. data rates) exceed current JLab experiments, they do not exceed the performance of other contemporary experiments.

The committee notes that although its members are comfortable with the choice of pipelined electronics and data-acquisition systems, development of a compact justification for this choice might be advisable in preparation for a Lehman review of GlueX

The decision to standardize all detector readout on a single TDC module design and a single Flash ADC module design is good, and will help simplify the overall electronics system design in a constructive way and conserve valuable engineering resources. The Committee feels that it is desirable to locate these modules in a radiation-free area if possible, in order to improve access. Such a location is also likely to provide a cleaner and better cooled environment, which will also improve reliability. The Committee does not feel that there is a compelling reason not to use a crate and bus based system for the electronic modules.

Are there any special areas of concern that deserve special study?

More manpower will be needed in order to fully realize the GlueX electronics system. Considerable special (technical) expertise will also be required.

The requirements and specifications of the analog front-end electronics are not yet adequately defined. This is coupled to the tentative status of some detector designs. The lack of full definition of detector designs may soon limit progress on electronics design, although there are other issues on which progress can presently be made. Some issues deserving attention now are listed under the "Milestones" section.

Does the collaboration have a sensible plan for management?

Rudiments of a plan for management of the electronics system exist, although the plan needs further development. The Committee suggests creating a single organization covering front-end electronics of all detector subsystems, trigger, data acquisition, and online software.

The electronics organization should be put in place during the development of the CDR, and the electronics management plan included in that document

Are their estimates of manpower needs realistic?

The manpower resources shown during the review will be inadequate for developing an electronics system of the scope required by GlueX. A bottoms-up estimate of the necessary manpower should be derived from the manpower requirements for development of the electronics chain for each electronics subsystem, including packaging, grounding, shielding, and power issues.

The committee anticipates that the GlueX collaboration will need to discuss support for additional electronics and computing manpower with Jefferson Lab and the funding agencies.

Do they have a realistic milestones as we prepare for the Lehmann review and beyond to construction?

The Committee estimates that a project of the overall scale of GlueX will require about 6 years to complete after CD-3 is achieved. Approximately two years are available between obtaining CD-0 and CD-3, during which the CDR must be developed and all groups involved in the construction of GlueX be put in place. This requires that by FY2006, all major R&D issues should have been addressed.

The current good work on the flash TDC and ADC should continue. A multichannel FADC needs to be designed, fabricated, and tested. The Committee takes note that multichannel testing has started on the FTDC, with encouraging results on cross-talk and time-slewing due to hits in neighboring channels which overlap in time. The collaboration is developing strategies to record all needed data online to correct such dependencies during offline analysis. High-speed, densely populated pipelined systems are known to have such coupling issues, and a strategy should be developed to address them for all electronics and detectors.

Analog front-end requirements deriving from the detector should be settled; a good first summary of this was exhibited to the Committee. The resulting specifications for the electronics should be settled and used to drive further R&D work. Prototype work on the needed front-ends will require about one year once these specifications are settled. This suggests a review of progress in this area by Jefferson Lab management around the beginning of FY2005, covering the status of analog designs and prototypes.

The collaboration has experience with the needed fast discriminators and has started to explore options for tracking chamber front-ends. A program to develop the tracking chamber front-ends, either from a new design or by adapting an existing design, for example from among the family of ASD-8 ASICs developed at U. Pennsylvania, needs to be mapped out soon by the collaboration.

There is a concept for a pipelined LVL-1 trigger as an integral part of the pipelined online system. The link work shown should be completed. The general concept of local sums at the front-end board level, followed by crate-level sums and subsequent transfer to a central Global LVl-1 processing area, is sound. A concept and proof-of-principle for crate backplane operation at the required high rate needs to be developed for the CDR. If high-speed serial operation proves challenging, the collaboration should explore possible parallel concepts to lower the bus-speed requirements. The global design concept for LVL-1 also needs to be developed for the CDR.

A concept for the timing system and trigger distribution system, as well as their synchronization (pipelined operation, exception injection), needs to be developed for the CDR. This should address establishing, maintaining and diagnosing the synchronization of the various pipelines. Similarly, a concept for the calibration system, and how it integrates with both the timing/trigger system as well as the analog front-ends and FADC/FTDC, needs to be prepared for the CDR.

The collaboration should start prototyping of the parallel event builder. Manpower needs to be identified at Jefferson Lab and elsewhere to carry this concept through to its execution. The LVL-3 concept is sound and the Committee applauds the opportunistic tests of it using CLAS. A concept for the software framework for algorithms needs to be established for the CDR as well as a method to test this using simulated events.

Finally, power management, grounding and shielding concepts need to be established for the CDR. These must address overall issues as well as those specific for each detector type. The Committee was pleased to hear the report about existing efforts in these areas at Jefferson Lab. GlueX is a large and complicated apparatus employing a demanding readout architecture, which in turn requires proper grounding and shielding be incorporated from the outset.

Are there any major items missing in their list of R&D tasks? Is the priority given to each appropriate at this stage?

The R&D tasks judged to be most pressing are noted above. It is critical that the choices made in readout architecture reflect requirements imposed by the physics and detector choices. We recommend that Jefferson Lab review the status of detector prototypes, with a key aspect of this review being the ability of each detector group to define their electronics needs. It is important to insure that the requirements on the electronics derive from the physics. For instance, momentum resolution requirements drive position resolution requirements, which drive time resolution requirements. Similarly, energy resolution

and trigger sum selectivity requirements for the calorimeter drive choices about the number of bits in flash circuits. It must always be kept in mind that requirements are distinct from achievable performance and specifications. The review suggested above should examine these points so that design time and construction cost may be minimized while needed physics performance is preserved.

One example of an area of concern is the choice of barrel calorimeter photosensors. Familiarity with the chosen sensor and its implications for electronics requirements should be demonstrated. The Committee notes that CMS and ALICE have chosen to use custom Hamamatsu avalanche photodiodes to read out both crystal and lead-scintillator calorimeters and have developed appropriately matched preamplifiers and shapers. These APDs have moderate gain, around 50, are fast, and operate at modest voltages of less than 100 volts. These devices need to be studied by the collaboration to see if they would match the proposed barrel calorimeter light output levels. The CMS and ALICE groups use over 200,000 of these photodiodes and CLAS has several hundred of them and can probably supply samples.

Another area of some concern is the technology choice for the vertex tracker, particularly since its physics requirements seem to be undergoing some reconsideration. Present ideas center on tracking fibers and dense arrays of photosensors, such as the VLPC sensor array developed at FNAL. There are issues of VLPC suitability and availability which must be addressed in a timely manner if the collaboration is to pursue this option. Further remarks concerning the VLPC system are given below. If only vertex finding is needed and the fiber solution proves overly challenging, the Committee asks whether a modest silicon-strip array would serve the purpose. Various electronics designs exist, notably at SLAC and FNAL for Tevatron and LHC use.

In many of the above remarks we have stressed the relative priorities between design and prototyping for various items. The collaboration may choose to be more ambitious than suggested, but the Committee feels the items noted should reach the state suggested before the CDR is deemed complete. Some of these efforts will likely require directed funding beyond present resources of the collaboration; thus a prioritized R&D program should be developed in consultation with Jefferson Lab and the funding agencies as soon as possible.

Are there technologies or developments which we have overlooked that may allow cost savings and/or improved technical performance?

The Collaboration should perform a systematic search for existing developments performed by other experiments that will facilitate the development

of the GlueX analog front-end electronics. Some examples of interesting developments include:

- For anode wire readout in drift chambers, the family of amplifier/shapers and amplifier/shaper/discriminators developed at the University of Pennsylvania. These are generally referred to as the ASD-8 family and have been used successfully in experiments (ATLAS and PHENIX) in which two of the Committee members currently participate. If the ASD-Q, presented at the meeting, is chosen, then a pipelined TDC capable of recording pulse width is a must. The TMC chip developed by Y. Arai of KEK, also used in different manners by ATLAS and PHENIX, should be investigated.

- The Fermilab design for VLPC readout should be investigated for use in the vertex trackers fiber readout. The collaboration should consider the availability of VLPCs and whether elements of the Fermilab readout system are applicable within the context of the system design of the GlueX electronics. These considerations should be addressed soon, because significant development work may be required for this subsystem.

- For the forward drift chambers, the amplifier/shapers developed for the ATLAS, CMS, and PHENIX cathode strip chambers might provide a solution for the analog front-end. These ASICs are designed for strips up to over 200 pF in one case. The speed and packaging requirements differ among these experiments, thus the collaboration would need to study their suitability for the GlueX chambers, once the parameters are sufficiently well determined.

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